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| EXAMINER | |
|---|---|
| VO, TED T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2191 | |

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/645,871 | OGAWA ET AL. | |
| | Examiner | Art Unit | |
| | Ted T. Vo | 2191 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is in response to the amendment filed on 08/21/2006.

Claim 12 is added. Claims 1-12 are pending in the application.

### *Response to Arguments*

2. In view of the amendment and arguments given in Remarks, filed on 8/21/06, Applicants' arguments to the rejections of 35 USC 112 second paragraph and the rejection under 35 USC 101 have been considered but not persuasive.

Regarding arguments of Claims 6, 11 under 112 second paragraph, it should be noted that Claims 6 and 11 remains being improper dependent claims because they fail to further limit the subject mater of the claims in which they depend. It appears Claims 6 and 11 are in independent form. It requires amending the claim in independent form. See MPEP 608(n).

Regarding the argument of claims 1-11 under 35 USC 101, see analysis provided in the rejection below.

Regarding the Applicant's arguments to the rejection under 35 USC 102, with respect to the newly added limitations "*wherein each of the constraints is whether a corresponding hardware resource is capable of processing an instruction and a succeeding instruction which is dependent on the instruction in parallel*", where Applicants reasoned that Palem only discloses generally that deciding the execution timing of the instruction is to be based on data dependencies and allocatable registers. It appears that Applicants regard the Palem execution's instruction is general (as emphasis added: in parallel). Examiner responds: The claim is mainly on: A priority calculation step, and an execution timing. As recited as Palem discloses having these features. Yes, Palem1 discusses a generic processor; however, he includes Superscalar RISC (p.8, box 47), which is not a uni-processor as argued. It is customary to describe a processor. It is known that in the modem computer system, the system is including parallel

execution. The general description therefore is inherent to the parallel system. The newly limitation in the claim simply only includes "in parallel", but there is no functionality to limit it for a difference from a generic computer system. The limitation in the claims remains including two features, "priority calculation" and "timing execution" as in every prior art's Instruction scheduling.

It should be noted that:

See MPEP § 2131.01.

**2131.01 Multiple Reference 35 U.S.C. 102 Rejections**

Normally, only one reference should be used in making a rejection under 35 U.S.C. 102. However, a 35 U.S.C. 102 rejection over multiple references has been held to be proper when the extra references are cited to:

(A) Prove the primary reference contains an "enabled disclosure;"
(B) Explain the meaning of a term used in the primary reference; or
(C) Show that a characteristic not disclosed in the reference is inherent.

See paragraphs I-III below for more explanation of each circumstance.

Furthermore, refer to MPEP 714.04, the amendment in this present application tend to includes "in parallel" without attempt to point Out Patentable Novelty. Accordingly, the action is made final. The Newly added reference aims to show inherency; how it is not necessary disused or detailed in a given reference.

***Claim Objections***

3. Claims 6 and 11 are objected to.

It should be noted that a dependent claim is to limit its independent claim. Claim 6 recites a program conversion method, and this scope is to describe a method independently from the method of Claim 1. Claim 6 shows as dependent to Claim 1 but does nothing to limit the Claim 1. This dependency is improper. Address the same to the rejection of Claim 11.

Convert into independent form is required.

***Claim Rejections - 35 USC § 101***

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. The claims 1-11 are rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

A claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47 USPQ2d at 1601-02.

As per Claims 1-6: It should be noted that claims 1-6 recite methods; therefore they are process claims. According to the requirement for statutory process claims, a claim must (A) result a physical transformation outside the computer for which a practical application in the technological arts is either disclosed in the specification or known by a skilled artisan, or (B) Computer-Related Processes Limited to a Practical Application in the Technological.

Claims 1-6 recite general processes. The Independent claims 1, 4 with recitations (a) calculating a priority of instructions, (b) deciding an execution timing do not result any thing in accordance to (A), nor substances defined as Computer-Related Processes. Therefore, the claims do not meet the statutory requirement.

As per Claims 7-8: Claims 7-8 recite a general device; the claims are classified as product claims. However, in order to be product claims like a machine, the claim must be "concrete thing" comprising "certain" device. The claims are a general device, i.e., the device covers, un-concrete thing. The claims have no concrete substances, or fail to define any substance to cause the device to be concrete.

As per Claims 9-10:Claims 9-10 are a computer program per-se "A computer-executable program", i.e. the claims are not a product or a process, but program per se. The body of the claims is only intended to an execution in a computer. Claiming program per se will be subject to 35 USC 101. Thus the claims remain rejected.

As per Claim 11: Claim 11 is an Abstract idea because of uncertainty of its claimed subject mater.

Claim 12 is statutory because it results a scheduling produced by a computer.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Palem et al., "Code Optimization in Mordern Compiler", http://www.cs.nyu.edu/courses/spring00/G22.3130-001/krishna_slides.pdf, 1998 (hereinafter: Palem1), "Scheduling Time-Constrained Instruction on Pipelined Processors", New York University, 2001 (hereinafter: Palem2).

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1: Palem discloses,

*An instruction scheduling method comprising:*

***a priority calculation step of calculating a priority of each of a plurality of instructions that are subjected to scheduling*** (Palem1: See page 13, rank function for prioritizing nodes – Palem2: see p. 82, sec 4, e.g. Compute ranks).

With regard this limitation:

***"based on dependencies between the plurality of instructions and constraints of hardware resources for processing the plurality of instructions,"*** (Palem1: See p. 5: Dependence Analysis)

***and***

***an execution timing decision step of deciding an execution timing of an instruction having a highest priority based on the priority of each of the plurality of instructions***, (Palem1: see p.9-12: show "Instruction Scheduling Algorithm", boxes 54-72, including box 59, Instruction Execution Timing; theses boxes discuss execution timing and latency problems, and Greedy. The discussion leads to the priority calculation of: A Critical Choice: The rank Function for Prioritizing Nodes. And thus it leads a decision based on calculating priority of the H(i) for how to choose a path in priority scheduling. See Palem2: p. 82, disclosing scheduling decision on in instructions in parallel (lines1-3), and show the Algorithm of computing timing constraints and create a priority list (e.g. a sequence of scheduling instructions), and based on timing constrains for secluding in parallel processors. And more importantly, see Palem1: p. 29: show Instruction Execution Timing is always associated with priority scheduling) ***wherein each of the constraints is whether a corresponding hardware resource is capable of processing an instruction and succeeding instruction which is dependent on instruction in parallel"***, (Palem1: p. 8: show the discussion is in a Superscalar RISC: a parallel processors. And the RISC is dealt with constraints corresponding to hardware resource of RISC parallel processors, where the dependent analysis that results a priority schedule is given in Palem1).

As per Claim 2: Palem discloses,

*The instruction scheduling method of claim 1, wherein* ***the dependencies being data dependency, anti-dependency, and output dependency*** (Palem1: refer to the analysis in boxes 40-42),

*the priority calculation step includes: a precedence constraint rank calculation substep of calculating a precedence constraint rank of each of the plurality of instructions, wherein (a) if the instruction has a succeeding instruction which is anti-dependent or output dependent on the instruction, the precedence constraint rank of the instruction is equal to a precedence constraint rank of the succeeding instruction, and (b) if the instruction has a succeeding instruction which is data dependent on the instruction, the precedence constraint rank of the instruction is higher than a precedence constraint rank of the succeeding instruction; and a resource constraint evaluation substep of judging (i) whether the instruction has a succeeding instruction which is dependent on the instruction, (ii) whether the instruction and the succeeding instruction have an equal precedence constraint rank, and (iii) whether a hardware resource*

*for processing the instruction cannot process the instruction and the succeeding instruction in parallel, and the priority calculation step raises the precedence constraint rank of the instruction and sets the raised precedence constraint rank as a priority of the instruction if all of the judgments (i), (ii), and (iii) are in the affirmative, and sets the precedence constraint rank of the instruction as the priority of the instruction if any of the judgments (i), (ii), and (iii) is in the negative.*

See all Figures in p. 13 associated with analysis in p. 7.

As per Claim 3: Palem discloses,

*The instruction scheduling method of claim 1, wherein the priority calculation step includes: a precedence constraint rank calculation substep of calculating a precedence constraint rank of each of the plurality of instructions, wherein (a) if the instruction has no succeeding instruction which is dependent on the instruction, the precedence constraint rank of the instruction is 1, (b) if the instruction has one or more succeeding instructions which are anti-dependent or output dependent on the instruction, the precedence constraint rank of the instruction is a highest one of precedence constraint ranks of the succeeding instructions, and (c) if the instruction has one or more succeeding instructions which are data dependent on the instruction, the precedence constraint rank of the instruction is a sum of 1 and a highest one of precedence constraint ranks of the succeeding instructions; and a resource constraint evaluation substep of calculating a resource constraint value of the instruction, by dividing a total number of instructions which are to be processed by a hardware resource for processing the instruction and whose execution timings have not been decided, by a maximum number of instructions that can be processed in parallel by the hardware resource, and the priority calculation step sets the resource constraint value as a priority of the instruction if the resource constraint value is larger than the precedence constraint rank, and sets the precedence constraint rank as the priority of the instruction if the resource constraint value is no larger than the precedence constraint rank.*

See all Figures in p. 13 associated with analysis in p. 7.

As per Claim 4: Programming language provides conditions for judging true, false of executed condition. For example "IF THEN ELSE" is always used in every computer language. Therefore, using "decision step", "redecision step" simply shows a body of a program, rather discussing a principle of an invention.

Accordingly, given references disclose programming languages to cover the teaching of claimed limitations:

*An instruction scheduling method for sequentially deciding execution timings of instructions that are subjected to scheduling, comprising: a decision judgment step of judging, after an execution timing of a first instruction is decided* (e.g. v2), *whether an execution timing of a second instruction can be decided so as to be within a predetermined time period* (e.g. v3 or v4, In this case, v4 falls in *a predetermined time period* ('Functional unit'), *based on a constraint of a hardware resource for processing the second instruction; and a redecision step of retracting, if the judgment of the decision judgment step is in the negative, the decision of the execution timing of the first instruction and deciding an execution timing of an instruction other than the first instruction*

(the instruction placed next to v2; in this case, is v4).

In light of the specification, the claim limitation falls in the performance of the Figures 169, 170, 171, 172, in p. 29, in combined with Fig 59, p. 10, where a sequence of instructions could be formed under a functional unit. The Figures show that after rank-performance (Figure 169), an instruction scheduling is judged based on constraints. It visually shows there are decisions causing the instruction scheduling to place v1, v2, v4, v3, v5, v6 in a sequence in accordance to Figure 172. It is clearly that the sequence is based on the execution timings of v1, v2, v3, v4, v5, v6, and the predetermined hardware resources (registers).

With regards to: *wherein the constraint is whether a resource constraint value of the second instruction is larger than a number of remaining clock cycles, the resource constraint value being calculated by dividing a total number of instructions which are to be processed by the hardware resource and whose execution timings have not been decided, by a maximum number of instructions that can be processed in parallel by the hardware resource* (See Palem1: box 63: Palem2. See p. 82, and refer to title "Pipelined Processors" for: *maximum number of instructions that can be processed in parallel by the hardware resource*).

As per Claim 5: Palem discloses, *The instruction scheduling method of claim 4, wherein the predetermined time period is expressed by a number of clock cycles, the decision judgment step includes: a resource constraint evaluation substep of calculating a resource constraint value of the*

*second instruction, by dividing a total number of instructions which are to be processed by the hardware resource and whose execution timings have not been decided, by a maximum number of instructions that can be processed in parallel by the hardware resource, and the decision judgment step judges in the negative if the resource constraint value is larger than the number of clock cycles* (See Figures 169, 172).

As per claim 6: With regards to, *A program conversion method characterized in that: an input program is converted to an object program including a plurality of instructions, and an execution timing of each of the plurality of instructions in the object program is decided using the instruction scheduling method of one of claim 1.* Palem's teaching is in compilation, where a compiler's input is a program and its output is an executable program, provided with register allocation, and instruction scheduling. Furthermore, see rationale addressed in Claim 1 above.

As per claim 7: See the rationale addressed in the rejection of Claim 1 above.

As per claim 8: See the rationale addressed in the rejection of Claim 4 above.

As per claim 9: See the rationale addressed in the rejection of Claim 1 above.

As per claim 10: See the rationale addressed in the rejection of Claim 4 above.

As per claim 11: See the rationale addressed in the rejection of Claim 1 above.

As per claim 12: See the rationale addressed in the rejection of Claim 1 above.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
October 27, 2006

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